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10/661,413	09/12/2003	Eric C. Saxe	15437-0579	6657

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,413	SAXE ET AL.	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-84 are presented for examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-84 are directed to non-statutory subject matter.

3. Claims 1, 13, and 26 are directed to a computer implemented method that lacks a tangible result. For example, the receiving of parametric information, construction of an abstraction, accessing an abstraction, nor determining whether to assign an execution thread to the PPM consist of a tangible result. Claims 2-12, 14-25, and 27-28 are rejected for being dependent upon rejected independent claims 1, 13, and 26.

4. Claims 29, 41, and 54 are directed to a computer readable medium that may take the form of a transmission media. According to page 30, [0064] of Applicant's Specification, Transmission media comprises coaxial cables, copper wire, and fiber optics, comprising the wires that comprise bus 902. Transmission media can also take the form of acoustic or electromagnetic waves, such as those generated during radio-wave, infra-red, and optical data communications. Said transmission media is not statutory subject matter and fails to fall under one of the four statutory categories of inventions. Claims 30-40 and 42-53 are rejected for being dependent upon rejected independent claims 29, 41, and 54.

5. Claims 57, 69, and 82 are directed to a system that could be interpreted to one of ordinary skill in the art as software, per se. The broadest reasonable interpretation of a physical

processing module could be interpreted as software, per se. Claims 58-68 and 70-81 are rejected for being dependent upon rejected independent claims 57, 69, and 82.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rashid (US 2005/0033831 A1) in view of Brenner et al. (hereinafter Brenner) (US 7,080,379), and further in view of Kimmel et al. (hereinafter Kimmel) (US 6,105,053).

7. As to claim 1, Rashid teaches a computer implemented method, comprising: receiving parametric information pertaining to a physical processing module (PPM) ([0009], [0012], Fig. 2A, items 210a-210h, etc.).

8. Rashid is silent in constructing an abstraction of the PPM based, at least partially, upon the parametric information, the abstraction comprising an indication of how many logical processing entities are provided by the PPM, the abstraction further comprising operational information indicating one or more operational characteristics of the PPM.

9. However, Brenner teaches a multiprocessor system that indicates how many logical processing entities (threads, data associated with threads, etc.) are provided by a processing unit for the purpose of being able to perform load balancing. One of ordinary skill in the art would

have known to modify Rashid's multiprocessing system such that it would include the feature of determining the load or how many logical processing entities (threads, data associated with threads, etc.) are provided by a processing unit. The suggestion/motivation for doing so would have been to be able to perform load balancing, and thus, improve the processing of the overall system.

10. Furthermore, Kimmel teaches a multiprocessor system containing a plurality of job processors with an operating system that utilizes software abstraction of the hardware architecture of the multiprocessor system so that there can be a close affinity between the processes and the job processor and that operational characteristics of the job processors could be represented in software (col. 1, lines 59-67, col. 2, lines 1-15, Abstract). One of ordinary skill in the art would have known to modify the multiprocessor system of Rashid in view of Brenner such that it would include the feature of utilizing data abstractions for the execution units so that representations could be made on information such as the number of logical processing entries. The suggestion/motivation for doing so would have been to increase system throughput, maintain a balanced processor load, and ensuring that processes do not languish in the system (col. 1, lines 59-67 and col. 2, lines 22-35).

11. Rashid, Brenner, and Kimmel are all in the same field of endeavor of multiprocessing with solving the same problem of load balancing. Therefore, it would have been obvious to one of ordinary skill in the art to combine Rashid, Brenner, and Kimmel to obtain the invention of claim 1.

12. As to claim 2, Rashid teaches wherein the operational information comprises an operating clock frequency for the PPM (page 3, [0051], lines 1-3).

13. As to claim 3, Rashid teaches wherein the operational information comprises an indication of a current load on the logical processing entities provided by the PPM ([0079], lines 20-21).

14. As to claim 4, Rashid teaches wherein the resource sharing information indicates whether a data pathway is being shared by at least some of the logical processing entities (same pathway to TLB or to cache, etc.) (page 6, [0081], page 3, [0051], Fig. 2A, items 214a-h or 212a-h).

15. As to claim 5, Rashid teaches wherein the resource sharing information indicates whether a translation lookaside buffer is being shared by at least some of the logical processing entities (page 6, [0081], page 3, [0051]).

16. As to claim 6, Rashid teaches wherein the resource sharing information indicates whether a physical processing core is being shared by at least some of the logical processing entities ([0066], [0099], [0123]).

17. As to claim 7, Rashid teaches wherein the operational information comprises resource sharing information indicating whether one or more resources on the PPM are being shared by at least some of the logical processing entities ([0066], [0099], [0123]).

18. As to claim 8, Rashid teaches wherein the resource sharing information indicates whether a cache memory on the PPM is being shared by at least some of the logical processing entities (Fig. 2A, items 214a-h or 212a-h).

19. As to claim 9, Brenner teaches further comprising: determining, based at least partially on the resource sharing information, a queue arrangement for use in assigning execution threads to one or more of the logical processing entities (col. 1, lines 24-47).

20. As to claim 10, Brenner (col. 1, lines 24-47) and Kimmel (col. 1, lines 59-67, col. 2, lines 1-15, Abstract) teach wherein the abstraction further comprises information indicating the queue arrangement.

21. As to claim 11, Brenner teaches wherein a single queue may be used to hold execution threads assigned to two or more of the logical processing entities, such that the two or more logical processing entities share the single queue (col. 1, lines 35-40, col. 2, lines 35-37).

22. As to claim 12, Kimmel (col. 1, lines 16-18) and Brenner (col. 2, lines 35-37) teach wherein the two or more logical processing entities share one or more resources on the PPM.

23. As to claim 13, it is rejected for similar reasons as stated in the rejection of claim 1.

24. As to claims 14-15, they are rejected for the same reasons as stated in the rejections of claim 2-3, respectively.

25. As to claim 16, it is rejected for the same reasons as stated in the rejection of claim 7.

26. As to claim 17, Rashid ([0123]), Brenner (see Abstract) and Kimmel (col. 13, lines 42-46)teaches in response to a determination to assign an execution thread to the PPM, determining, based at least partially upon the resource sharing information, to which of the logical processing entities to assign the execution thread.

27. As to claim 18, it is rejected for the same reasons as stated in the rejection of claim 4.

28. As to claims 19-21, they are rejected for the same reasons as stated in the rejections of claim 4-6, respectively.

29. As to claim 22, Rashid ([0123]), Brenner (see Abstract) and Kimmel (col. 13, lines 42-46) teaches wherein the abstraction further comprises information indicating a queue arrangement for use in assigning execution threads to one or more of the logical processing entities, wherein the queue arrangement indicates a particular queue assigned to two or more of the logical processing entities such that the two or more logical processing entities share the queue, and wherein the method further comprises:

30. assigning an execution thread to the particular queue for processing by one of the two or more logical processing entities.

31. As to claim 23, it is rejected for the same reasons as stated in the rejection of claim 12.

32. As to claim 24, Rashid ([0078], [0100]) and Kimmel (col. 19, lines 1-21, Abstract) teach wherein the abstraction further comprises a storage location for a pointer to a hardware specific routine comprising at least scheduling instruction, and the method further comprises scheduling execution threads according to the scheduling instructions.

33. As to claim 25, it is rejected for the same reasons as stated in the rejection of claims 2-4. In addition, Kimmel teaches the use of the dispatcher (see Abstract, col. 2, lines 36-46).

34. As to claim 26, it is rejected for the same reasons as stated in the rejection of claim 1. In addition, Rashid teaches a plurality of PPMs that are used ([0009], [0012], Fig. 2A, items 210a-210h, etc.). Finally, Rashid teaches that each PPM/core can execute different software programs and routines, and even run different operating systems ([0064]).

35. As to claim 27, Rashid ([0066], [0094]) and Kimmel (col. 1, lines 59-67 though col. 1-20) teaches wherein the first PPM comprises a first physical processing core which supports a single hardware thread, wherein the second PPM comprises a second physical processing core which supports a plurality of hardware threads, wherein constructing the first abstraction

comprises indicating the first physical processing core as a single logical processing entity, and wherein constructing the second abstraction comprises indicating the second physical processing core as a plurality of logical processing entities.

36. As to claim 28, Rashid ([0066], [0094]), Brenner (col. 1, lines 24-47), and Kimmel (col. 1, lines 59-67 though col. 1-20) teaches wherein constructing the second abstraction comprises indicating that the plurality of logical processing entities corresponding to the second physical processing core share one or more resources of the second PPM.

37. As to claim 29, it is rejected for the same reasons as stated in the rejection of claim 1.

38. As to claims 30-40, they are rejected for the same reasons as stated in the rejections of claim 2-12, respectively.

39. As to claim 41, it is rejected for the same reasons as stated in the rejection of claim 13.

40. As to claims 42-43, they are rejected for the same reasons as stated in the rejections of claim 2-3, respectively.

41. As to claims 44-53, they are rejected for the same reasons as stated in the rejections of claim 16-25, respectively.

42. As to claim 54, it is rejected for the same reasons as stated in the rejection of claim 26.

43. As to claims 55-56, they are rejected for the same reasons as stated in the rejections of claim 27-28, respectively.

44. As to claim 57, it is rejected for the same reasons as stated in the rejection of claim 1. In addition, Kimmel discloses that the operating system acts as the abstraction manager of the hardware architecture (col. 2, lines 58-67).

45. As to claims 58-68, they are rejected for the same reasons as stated in the rejections of claim 2-12, respectively.

46. As to claim 69, it is rejected for the same reasons as stated in the rejection of claim 1 and/or 13.

47. As to claims 70-71, they are rejected for the same reasons as stated in the rejections of claim 2-3, respectively.

48. As to claim 72, it is rejected for the same reasons as stated in the rejection of claim 4.

49. As to claim 73, Kimmel teaches wherein in response to a determination to assign an execution thread to the PPM, the dispatcher determining, based at least partially upon the

resource sharing information, to which of the logical processing entities to assign the execution thread (Abstract, col. 2, lines 36-46).

50. As to claim 74, it is rejected for the same reasons as stated in the rejection of claim 8.

51. As to claims 75-77, they are rejected for the same reasons as stated in the rejections of claims 4-6, respectively.

52. As to claim 78, it is rejected for the same reasons as stated in the rejections of claim 9 and 10.

53. As to claim 79, Rashid ([0123]) and Kimmel (Abstract) teach wherein the two or more logical processing entities share one or more resources on the PPM.

54. As to claims 80-81, they are rejected for the same reasons as stated in the rejections of claim 24-25, respectively.

55. As to claim 82, it is rejected for the same reasons as stated in the rejection of claim 26. In addition, Kimmel discloses that the operating system acts as the abstraction manager of the hardware architecture (col. 2, lines 58-67).

56. As to claims 83-84, they are rejected for the same reasons as stated in the rejections of claim 27-28, respectively.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Drysdale et al. (US 2003/0084269 A1)** discloses synchronizing and communicating between processing entities, such as cores or threads, in a multiprocessor (see Abstract, [0013]).
- **Tanabe (JP 2004171167)** discloses a multiprocessing that allocates threads based on a number of threads of a processor (see Derwent Abstract).
- **Smith (US 2004/0024874 A1)** discloses a multiprocessing system that determines the load of each processing unit for load balancing purposes (see Abstract).
- **Boggs et al. (US 7,051,329 B1)** discloses a multithreaded processor and the management of resources based on the number of threads currently executing that concurrently changes (see Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Kenneth Tang/
Examiner, Art Unit 2195